IN THE SPECIFICATION

Please amend the specification as follows:

1. Amend paragraph [0002] as follows:

--The present invention relates to a semiconductor integrated circuit capable of testing a memory, in particular testing a memory having a redundant cell and testing a peripheral logic of the memory, using a Built In Self Test (BIST), and ~~an~~ a test method thereof.--

2. Amend paragraph [0014] as follows:

--The present invention is made so as to solve above problems, and the object thereof is to provide a semiconductor integrated circuit which can suppress an increase in circuit area for redundant repair and circuit area for scan test, and ~~an~~ a test method thereof.--

3. Amend paragraph [0019] as follows:

--a first data storage section, which during ~~an~~ a test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said

comparing section as faulty address data, and during ~~an~~ a test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory;--

4. Amend paragraph [0028] as follows:

--a first data storage section, which during ~~an~~ a test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said comparing section as faulty address data, and during ~~an~~ a test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory; and--

5. Amend paragraph [0037] as follows:

--a first data storage section, which during ~~an~~ a test of said memory, retrieves all Row address signals or a signal which has branched a part of bits therefrom inputted into said memory from said test pattern generating section as faulty address data, and during ~~an~~ a test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain;--

6. Amend paragraph [0045] as follows:

--a first data storage section, which during ~~an~~ a test of said memory, retrieves all Row address signals or a signal which has branched a part of bits therefrom inputted into said memory from said test pattern generating section as faulty address data, and during ~~an~~ a test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain; and--

7. Amend paragraph [0052] as follows:

--a first data storage section, which during ~~an~~ a test of said memory, retrieves a signal which has been branched from an address signal inputted into said memory from said test pattern generating section, and an output signal from said comparing section as faulty address data, and during ~~an~~ a test of a peripheral logic of said memory, is used for observing the input signal into said memory as a part of the scan chain;--

8. Amend paragraph [0057] as follows:

--~~An~~ A test method of a semiconductor integrated circuit of the present invention characterized in that it is ~~an~~ a test method of the semiconductor integrated circuit configured as described above; and the first data storage section is used for

retaining fault information on the memory when inspecting the memory, and is used for observing an input signal into the memory when inspecting the peripheral logic of the memory.--

9. Amend paragraph [0128] as follows:

--In order to perform the repair for the memory 604 in the Row direction, information on a Row address of a cell with fault is needed for identifying a Row line with fault. Symbol 605 represents a first data storage section, which during ~~an~~ a test of the memory 604, retrieves all Row address signals or a signal, in which a part of bits has branched therefrom, inputted into the memory 604 from the test pattern generating section 601 as the faulty address data. That is, when performing the repair processes for the memory 604, the Row address of the cell with fault is stored, a Row address of a faulty cell detected first is stored, and the value is retained in the first data storage section 605 after that. In order to hold the data stored in the first data storage section 605, the value retained in the second data storage section 606 is used. If the second data storage section 606 has a value showing a state after detecting the first failure, the value stored in the first data storage section 605 is kept retaining. Moreover, when performing the scan test for the peripheral logic of the memory 604, the first data storage

section 605 configures a part of the scan chain and is used for observing the failure which is transmitted to the memory 604, so that the failure detection of the peripheral logic of the memory 604 can be improved.--

10. Amend paragraph [0174] as follows:

--In order to perform the repair for the memory 1004 in the Column direction and the Row direction, information on a Column address and its bit location of a cell with fault, and on a Row address are needed for identifying a Column line with fault and a Row line with fault. Symbol 1005 represents a first data storage section, which during ~~an~~ a test of the memory 1004, retrieves a signal which has branched from address signals inputted into the memory 1004 from the test pattern generating section 1001, and an output signal from the comparing section 1002 as the faulty address data. That is, when performing the repair processes for the memory 1004, the information on the Column address and its bit location of the cell with fault, and that on the Row address are stored.--